WHAT IS CLAIMED IS:

1. A multilayer-wiring substrate comprising:

a first wiring conductor with a recessed surface formed by etching a surface of the first wiring conductor,

a first insulating layer formed on a surface of the first wiring conductor except over the recess so that a first via-hole penetrates through the first insulating layer to the recessed surface; and

a second insulating layer formed on the other surface of the first wiring conductor.

2. A multilayer-wiring substrate as claimed in claim 1, further comprising:

a first via-conductor plated on an inner peripheral wall of the first via-hole and extendingly plated on the recessed surface of the first wiring conductor that forms a bottom of the via- hole; and

a second wiring conductor formed on the first insulating layer and extendingly connecting with the first via-conductor.

3. A multilayer-wiring substrate as claimed in claim 2, further comprising:

a third insulating layer formed on the first insulating layer and on the second wiring conductor;

a second-via hole penetrating through the third insulating layer;

a second via conductor plated on a inner peripheral wall of the

second via-hole;

and a third wiring conductor formed on the third insulating layer and extendingly connecting to the second via-conductor,

wherein the second wiring conductor has a recessed surface on which the second via conductor is formed by plating, the recessed surface being formed by etching.

4. A multilayer-wiring substrate as claimed in claim 1, further comprising:

a solder bump adhering to the recessed surface of the first wiring conductor and formed in the first via-hole.

5. A multilayer-wiring substrate comprising:

a first wiring conductor having top and bottom surfaces; a first insulating layer formed on the top surface of the first wiring conductor; a first via-hole penetrating through the first insulating layer; and a first columnar via-conductor formed in the via-hole,

wherein the first wiring conductor has a first recessed surface formed at the top surface of the first wiring conductor so that a bottom end of the first columnar via-conductor contacts the first recessed surface of the first wiring conductor.

6. A multilayer-wiring substrate as claimed in claim 5, further comprising:

a second wiring conductor formed on top of the first insulating layer and extendingly forming a top end of the first columnar via-conductor; a second insulating layer formed on the top surface of the second wiring conductor; a second via-hole penetrating through the second insulating layer to the second wiring conductor; and a second columnar via-conductor formed in the via-hole,

wherein the second wiring conductor has a second recessed surface in alignment with the end surface of the first columnar via-conductor so that an end of the second columnar via-conductor contacts the second recessed surface of the second wiring conductor.

7. A multilayer-wiring substrate as claimed in claim 6, further comprising:

a third wiring conductor formed on top of the second insulating layer and extendingly forming an end of the second columnar via-conductor formed in the second via-hole; a third insulating layer covering the third wiring conductor; and a third via-hole penetrating through the third insulating layer,

wherein the third wiring conductor extendingly forming the end of the second columnar via conductor has a third recessed surface for soldering a solder bump to be formed in the third via-hole.

8. A multilayer-wiring substrate as claimed in claim 1, wherein the insulator comprises a material selected from the group

consisting of resin, glass, ceramic and mixtures thereof.

9. A multilayer-wiring substrate as claimed in claim 1, further comprising:

at least one of gold and nickel plated on the recessed surface of the wiring conductor.

10. A multilayer-wiring substrate as claimed in claim 1, further comprising:

a columnar via-conductor formed in a via hole that penetrates at least two insulating layers, the via-conductor having a recessed end surface positioned in the via-hole.

11. A multilayer-wiring substrate as claimed in claim 1, wherein a depth of the recess is 5-30 % of the thickness of the wiring conductor.

12. A multilayer-wiring conductor as claimed in claims 1, wherein all of said conductors comprise copper.

13. A method for fabricating a multilayer-wiring substrate having a via-conductor in a via-hole, comprising:

forming an insulating layer on a wiring conductor; forming a via-hole in the insulating layer by removing the insulating layer to an extent that the insulating layer in the via-hole becomes fragmented and

adheres to the wiring-conductor located at the bottom of the via-hole; then etching the wiring conductor located at the bottom of the via-hole so that the fragments are removed and a recess is formed in the conductor; and then forming a via-conductor in the via-hole by plating a metal on an inner peripheral wall of the via-hole and extendingly plating the metal on a surface of the recessed portion of the wiring conductor.

14. A method for fabricating a multilayer-wiring substrate having a via-conductor in a via-hole as clamed in claim 13, further comprising:

etching an inner peripheral wall of the via-hole that penetrates the insulating layer before etching the wiring conductor located at the bottom of the via-hole.

15. A method for fabricating a multilayer-wiring substrate, comprising the steps of:

forming a photosensitive resin layer on a metal-wiring conductor;

exposing the photosensitive resin layer and then developing to form a via-hole therein;

chemically etching resin at a surface of the photosensitive resin layer and resin at an inner wall of the via-hole; and

chemically etching a surface of the metal-wiring conductor exposed at a bottom of the via-hole so as to form a recessed surface at the surface of the metal-wiring conductor.

16. A method for fabricating a multilayer-wiring substrate as claimed in claim 15, wherein the step of etching the surface of the metal-wiring conductor comprises etching the surface of the metal-wiring conductor in an amount of 5-30% of the thickness of the metal-wiring conductor.

17. A method for fabricating a multilayer-wiring substrate as claimed in claim 15, wherein said developing comprises holding the multilayer-wiring substrate substantially horizontally and turning the substrate upside down during the development so that a via-hole axis is formed perpendicular to the recessed surface of the metal wiring conductor.